WE CLAIM:

1. A signal strength indicator circuit, comprising:

a signal input for receiving an input signal;

a set of rectifiers including an asymmetric switching pair of rectifiers for providing an output signal that is inversely proportional to the input signal, wherein a first side of the asymmetric switching pair is operably connected to a power supply through a resistor; and

a signal output for outputting the output signal.

2. The circuit of claim 1, wherein a second side of the pair of rectifiers is operably connected directly to the power supply.

3. The circuit of claim 2, wherein, when the circuit is in operation, the second side of the asymmetric switching pair of rectifiers emits the output signal.

4. The circuit of claim 1, further comprising a set of amplifiers that are operably connected to the set of rectifiers.

5. The circuit of claim 1, further comprising a comparator circuit that is operably connected to the set of rectifiers.

6. The circuit of claim 1, wherein the signal input is configured to receive a first portion of the input signal from a first mixer and a second portion of the input signal from a second mixer.

7. The circuit of claim 6, wherein the signal input is configured to receive the first portion and the second portion of the input signal,

and wherein the first portion and the second portion are 90° out of phase with each other.

8. A method of processing a signal received by a signal strength indicator circuit, the method comprising the steps of:

receiving an input signal;

rectifying the input signal through a set of rectifiers that includes an asymmetric switching pair of rectifiers to generate an output signal that is inversely proportional to the input signal;

stabilizing the output signal by operably connecting a first side of the asymmetric switching pair to a power supply through a resistor; and

outputting the output signal.

9. The method of claim 8, further comprising the step of:

stabilizing the output signal versus process variations by operably connecting a second side of the asymmetric switching pair directly to the power supply.

10. The method of claim 9, wherein the rectifying step comprises generating the output signal at the second side of the asymmetric switching pair.

11. The method of claim 8, further comprising the step of amplifying the input signal through a set of amplifiers.

12. The method of claim 8, further comprising the step of comparing the output signal to at least one threshold value.

13. The method of claim 12, wherein the comparing step further comprises comparing the output signal to at least two threshold values using the comparator circuit.

14. The method of claim 8, wherein the receiving step comprises receiving a first portion of the input signal from a first mixer and a second portion of the input signal from a second mixer.

15. The method of claim 14, wherein the receiving step comprises receiving the first portion and the second portion of the input signal, and wherein the first portion and the second portion of the input signal are 90° out of phase with each other.

16. A signal strength indicator circuit, comprising:

receiving means for receiving an input signal;

rectifying means for providing an output signal that is inversely proportional to the input signal, the rectifying means including an asymmetric switching pair of rectifiers operably connected on a first side thereof to a power supply through a resistor; and

outputting means for outputting the output signal.

17. The circuit of claim 16, wherein the asymmetric switching pair of rectifiers included in the rectifying means is operably connected, on a second side thereof, directly to the power supply.

18. The circuit of claim 16, further comprising amplifying means for amplifying signals in the circuit, wherein the amplifying means are operably connected to the rectifying means.

19. The circuit of claim 16, further comprising comparing means for comparing the output signal to at least one threshold value, wherein comparing means are operably connected to the rectifying means.

20. The circuit of claim 16, wherein the receiving means is configured to receive a first portion of the input signal from a first mixer and a second portion of the input signal from a second mixer.